Application of Timing Variation Modeling to Speedpath Diagnosis

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***Abstract*—The impact of timing variations on the performance of *Very-Large-Scale Integrated* (VLSI) circuits is increasing as the feature sizes shrink down into the nanometer scale. Timing variations induced by process, environmental or other effects may lead to a failing speedpath. In this paper, first a functional model of circuit timing is constituted. Then, timing variations are added to the model. Afterwards, this model is utilized to diagnose failing speedpaths.**

***Keywords*—diagnosis, speedpath, timing variation**

I. Introduction

Diagnosis of failing speedpaths is a major challenge in developing VLSI circuits as timing variations induced by process and environmental effects increase. A path which limits the frequency of a circuit is called a *speedpath* [1] [2]. A speedpath that fails timing constraints at the post-silicon stage is called *failing speedpath* [3].

The correct behavior of a circuit is verified at the stage of post-silicon validation by applying test vectors to the chip. when an error is detected, the debugging starts to diagnose root causes of the error. But this process is often a manual task which consumes a significant portion of the IC development cycle. Therefore, automated debugging approaches are necessary to speed up this process.

In the recent years, due to statistical variations imposed by process variations, *Statistical Static Timing Analysis* (SSTA) methods have been proposed [4]. SSTA methods analyze timing behavior of a circuit under statistical variations. A formal procedure based on integer linear programming is presented in [3] to diagnose segments of failing speedpaths. A variational model obtained from parameterized static timing analysis is used in [5] to create a cost function. Then, a branch and bound approach using this cost function determines probable failing speedpaths.

An approach based on trace buffers is presented in [6] to debug failing speedpaths. Trace buffers are used as a hardware structure to provide real-time observability to speedpaths during the normal operation of a chip. A scan-based hardware structure is used in [7] to debug failing speedpaths. The approach explores debug techniques based on at-speed scan test patterns. Failing traces are analyzed at slower-than-nominal clock frequencies in [8] to enhance the diagnosis resolution. In [9], failing speedpaths are isolated by applying clock shrinking on a tester and using a CAD methodology. The work in [10] models the timing behavior of a circuit and timing variations in a functional domain. The model is used to analyze the functional behavior of a circuit under timing variations.

In this paper, we utilize the timing variation model of [10] to diagnose failing speedpaths. First, the timing behavior of a circuit is converted into a functional domain based on a discrete model of time units. Modeling the timing behavior of a circuit in the functional domain allows the formal methods to comprehensively analyze the timing effects of a circuit. Timing variations are also modeled varying the value of a signal by an accuracy of one time unit. Given an erroneous trace obtained from a testbench, the created model is constrained to the erroneous trace in order to diagnose failing speedpaths. Our approach uses a SAT solver as an underlying engine.

The remainder of this paper is organized as follows. Our diagnosis approach is presented in Section II. Section III presents experimental results on benchmark circuits. The last section concludes the work.

II. Approach

At the post-silicon stage, test vectors are applied to the chip and the clock period is reduced to detect the erroneous effects of timing variations. This step is called clock shrinking. The erroneous behavior of timing variations is observed on registers or outputs. An error is detected by comparing the output values of the chip with the nominal output values obtained from simulation at the specified clock period. The test vectors activating timing variation and the erroneous output constitute an *Erroneous Trace* (ET).

Given an erroneous trace obtained from the testbench due to timing variations, our goal is to diagnose failing speedpaths, i.e., to determine which speedpaths have failed due to a timing variation. In the approach, a chip is validated in a testbench using clock shrinking and test vectors. The output of the testbench is an erroneous trace.

To debug a circuit, first a *Time Accurate Model* (TAM) of the circuit is constructed according to a time unit. The TAM is

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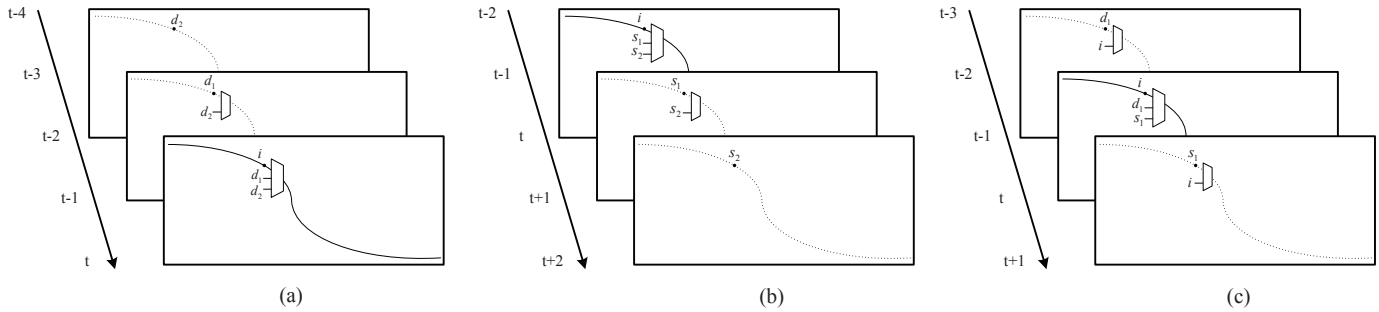

Fig. 1. (a) Slowdown (b) Speedup (c) Slowdown and Speedup

used in [10] to analyze the functional behavior of logic circuits under timing variations. The time unit specifies the diagnosis accuracy of the approach. To construct the TAM, first all gates are converted to *untimed gates*. Each untimed gate has a delay of one time unit. Buffers are inserted at the output of each original gate in order to convert an original gate to an untimed gate. After this step, all components in the circuit have a delay of one time unit. The new circuit is called *untimed circuit*. A TAM circuit is constructed from an untimed circuit. The underlying idea to construct a TAM is to use copies of a gate to represent the value of a gate at different points in time. Therefore, if an untimed gate is exercised several times at different time steps (e.g. due to reconvergent fanout), one copy of the untimed gate in each related time step is created. Having an erroneous trace and a TAM circuit, the diagnosis process starts to find failing speedpaths.

In this case, timing variations are added into the model. Timing variation may increase the component delay called slowdown, or may decrease the component delay called speedup. To model maximum timing variation V, V additional copies of the TAM are created. Figure 1 shows modeling timing variations when $V = 2$. Then, multiplexers are added to the TAM gate outputs to model timing variations by selecting the signal values from different time steps. Figure 1(a) shows modeling of slowdown. Speedup modeling is shown in Figure 1(b). Figure 1(c) is used for both slowdown and speedup. In Figure 1, values d_1 and d_2 denote a slowdown of one time unit and two time units for value of signal i. Values s_1 and s_2 denote a speedup of one time unit and two time units for value of signal i. The select lines of multiplexers are controlled by a constraint v. First v is 1. In this case, the inputs and outputs of the TAM is constrained to the erroneous trace ET and the diagnosis answers the following question: If there is a timing variation of one time unit, can the erroneous behavior of the corresponding ET be observed on the outputs? If there is no solution, the diagnosis function increases v. This process repeats until v reaches the maximum timing variation V.

The output of the diagnosis process is a set of fault candidates FCs. Each fault candidate includes the spatial and temporal information of a gate. All fault candidates together show failing speedpaths. Then, these failing speedpaths are visualized on the schematic view of the circuit.

III. Experimental Results

In this section, we evaluate our diagnosis approach empirically to debug the logic circuits under timing variations. The experiments are carried out on a Quad-Core AMD Phenom(tm) II X4 965 Processor (3.4 GHz, 8 GB main memory) running Linux. We use the combinational circuits of the ISCAS'85 benchmark suite to evaluate our approach. We synthesize our circuits using Synopsys Design Compiler with Nangate 45nm Open Cell Library [11].

The TAM-based diagnosis described in this paper is implemented using C++ in the WoLFram environment [12]. For the experiments, one time unit is $0.01\ ns$. MiniSAT is used as underlying SAT solver [13].

The simulation testbench is implemented using Verilog in ModelSim environment. Single slowdown faults of one time unit are injected in the circuit. Random test vectors are used in order to detect a slowdown in our testbench. Then, the erroneous trace is debugged by the approach.

Table I presents the experimental results. The table shows the circuit name (first column), the total number of gates (#Gates), the required run time in CPU seconds (Time), and the final number of fault candidates (#FC). Each fault candidate indicates that if a slowdown of one time unit at the appropriate time step on the output of the corresponding gate occurs, the erroneous behavior of the ET is created. The number of fault candidates (#FC) indicates the diagnosis accuracy of the diagnosis approach. A smaller number of #FC indicates a higher accuracy.

The second column in the table shows the total number of gates in the original circuit. By inserting buffers at the output of the original gates, it is converted to an untimed circuit. The total number of gates in the untimed circuits is shown in the third column. Afterwards, the TAM circuit is constructed. The fourth column shows the total number of gates in the TAM circuits. The required time to construct the TAM, to do diagnosis, and the total time are shown in columns five through seven.

TABLE I
TAM-BASED DEBUGGING

Circuit	#Gates when Time Unit = 0.01ns			Time (s)			#FC
	Original	Untimed	TAM	TAM	DBG	Total	
c17	6	26	35	0	194.97	194.97	2
c432	115	511	15446	135.01	1473.17	1608.18	20
c499	179	840	4358	4.6	212.58	217.18	2
c880	172	814	6483	14.95	1258.92	1273.87	17
c1355	238	1112	14338	93.33	2024.13	2117.46	26
c1908	142	658	5171	6.68	260.5	267.18	3
c2670	280	1296	8817	35.28	1391.03	1426.31	19
c3540	391	1792	50664	2347.64	1010.63	3358.27	10
c5315	632	3042	18283	290.24	1158.21	1448.45	16
c7552	772	3657	58468	3240.66	2093.9	5334.56	21

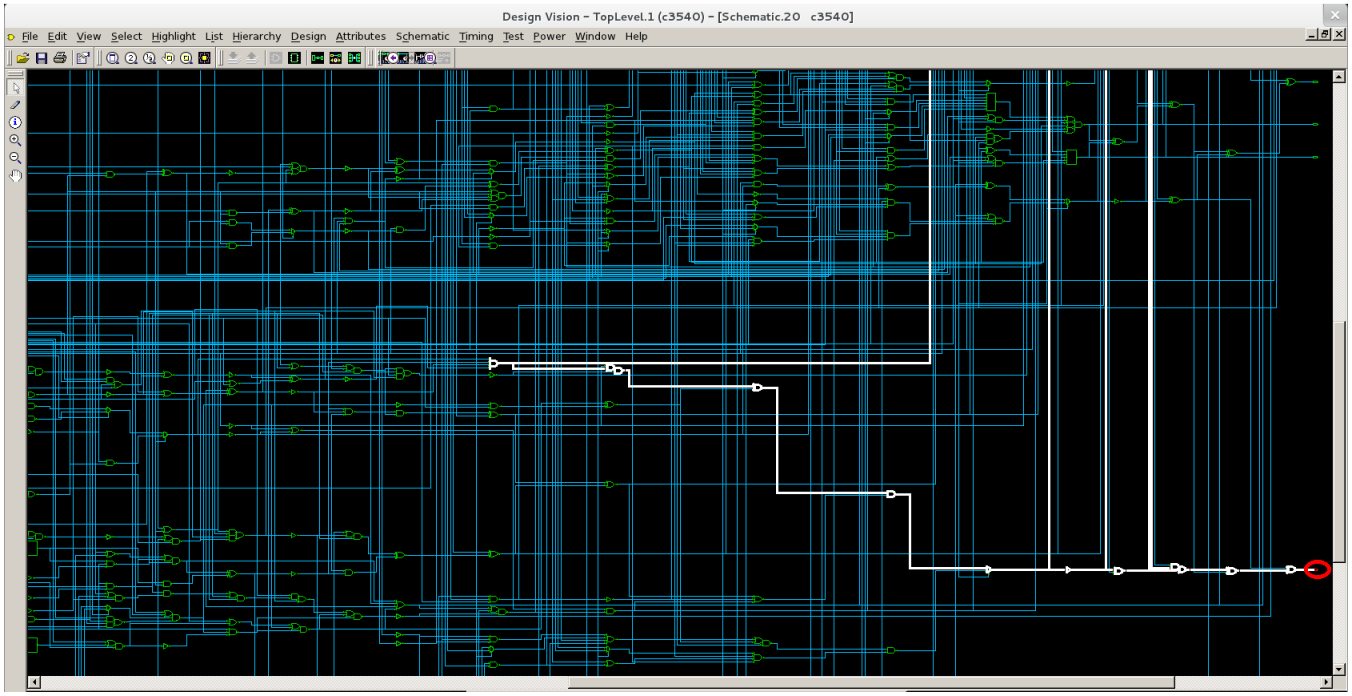

Fig. 2. Failing speedpath in circuit c3540

For circuit c432, the number of TAM gates is 15446, while the number of TAM gates is 4358 for circuit c499. This shows that in c432 there are more reconvergent fanouts in comparison to c499. The reconvergent fanouts increase the size of the TAM. The number of fault candidates for c432 is 20, while the number of fault candidates for c499 is 2.

In our experiments, all fault candidates together highlight failing speedpaths or some segments of failing speedpaths. Each fault candidate includes the location and the time of fault activation.

For circuit c3540, there are 10 fault candidates. They are visualized on the schematic view of the circuit in Figure 2 using *Synopsys Design Vision* [14]. The gates highlighted in white color show a segment of a speedpath which has violated the timing constraint. The red circle shows the output on which the error was observed. The approach was also applied to sequential circuit s298 from the ISCAS'89 benchmark suite. In this case, the erroneous behavior may be observed on internal registers of the circuit. Figure 3 shows the failing speedpath for the sequential circuit s298. The red circle shows a flipflop on which the error was observed. As the experiments show, our approach achieves a high diagnosis accuracy and can automatically extract failing speedpaths.

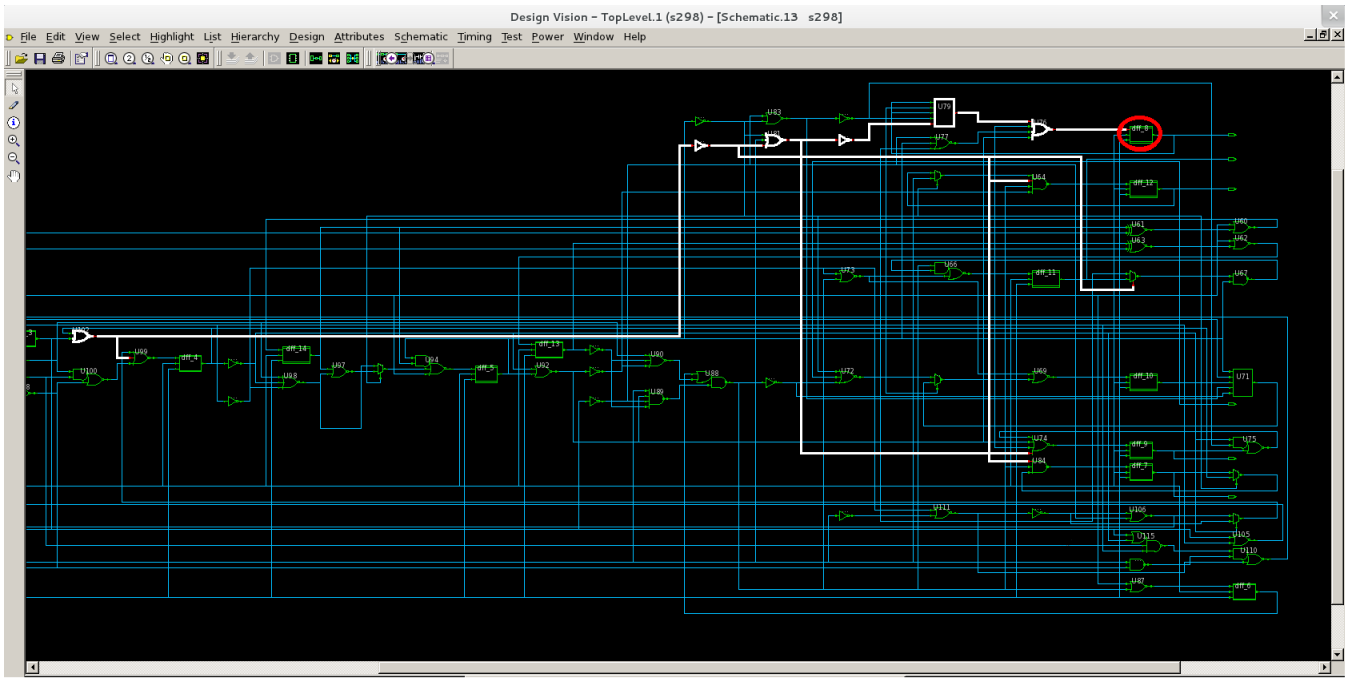

Fig. 3. Failing speedpath in circuit s298

IV. Conclusion

We presented an approach to diagnose speedpaths in logic circuits under timing variations. In the approach, first the timing behavior of a circuit is converted into the functional domain under a discrete model of time unit. Then, timing variation models are inserted into the functional domain. Afterwards, our diagnosis approach finds potential fault candidates including their spatial and temporal information.

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